

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Appl. No. : 10/787, 119
Applicant : Joerg Vollrath et al.
Filed : February 27, 2004
TC/A.U. : 2818
Examiner : Joerg Vollrath
Confirmation No. : 5078
Docket No. : 3000.0034C
Customer No. : 054500
Title : Integrated Semiconductor Circuit Having a Cell Array Having a Multiplicity of Memory Cells

Mail Stop Issue Fee

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

ISSUE FEE TRANSMITTAL

Transmitted herewith is an Issue Fee Transmittal (Form PTOL 85b) for the above-identified application.

Also enclosed is:

Other: Submission of Replacement Drawings including 1 sheet of drawings

Fees:

Issue Fee of \$1400.00
 Other Fees: \$300.00 for Publication Fee.

Total fee: \$1700.00

Payment of Fees:

Check No. 9265 in the amount of \$1700.00 for the total fee is attached.

Please charge \$____ to Deposit Account No. 05-0460 for the total fee. This paper is being submitted in duplicate.

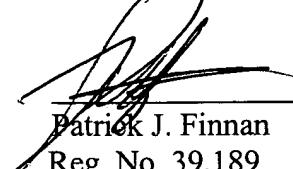
The Commissioner is hereby authorized to charge any additional fees that may be required, and to credit any overpayment, to Deposit Account No. 05-0460.

Dated: 12/02/2005

EDELL, SHAPIRO & FINNAN, LLC
CUSTOMER NO. 054500
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Respectfully submitted by
EDELL, SHAPIRO & FINNAN, LLC

By:


Patrick J. Finn
Reg. No. 39,189



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SUBMISSION OF REPLACEMENT DRAWINGS

Sir:

Enclosed is one sheet of replacement Figures in which Fig. 2 has been labeled "prior art".

It is believed no new fees are required. The Commissioner is hereby authorized to charge any additional appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 05-0460.

Dated: 12/02/05

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